New Simple Digital Self-Calibration Technique for Pipeline ADCs using the Internal Thermal Noise

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***Abstract*—This paper describes a new digital-domain self-calibration technique for high-speed pipeline A/D converters using the internal thermal noise as input stimulus. This low-amplitude noise is amplified and recycled by the ADC itself and, due to the successive foldings, it is naturally converted into uniform noise. This noise is then used to calculate the required calibrating-codes. As an example, the calibration of a 13-bit pipeline ADC shows that the overall linearity can be significantly improved using this technique.**

I. INTRODUCTION

High-resolution analogue-to-digital converters (ADCs) with sampling rate (F_S) in the range of 40 to 160 MS/s are required in a broad area of high performance applications, such as high-quality imaging systems, radar, modern wireless communications and short-distance data transmission over twisted-pair lines (VDSL2). These ADCs usually employ pipelining to relax the speed requirements of the analogue components. The precision is normally limited by the front-end stage of the pipeline, which must exhibit the accuracy of the overall ADC.

Without trimming or self-calibration, the overall resolution of these ADCs is limited by the gain and non-linearity errors of the front-end multiplying digital-to-analogue converter (MDAC). Linearity is limited to 10 bits by the component matching accuracy of most CMOS processes available today. As trimming is expensive, self-calibration, either in the analogue or in the digital domain, is employed by most ADC manufacturers.

Analogue techniques require calibration DACs and precision analogue components [1, 2]. Digital calibration avoids the use of sophisticated analogue circuitry, but puts an extra burden on the digital part of the ADC [3, 4]. Furthermore, the MDAC of a calibrated stage requires additional switches to perform the code error measurements [4]. The technique proposed in [3] can only be employed in 1.5-bit MDACs, which prevents the use of multi-bit front-end stages to obtain more energy-efficient ADCs [5].

A histogram-based technique, illustrated in Fig. 1(a) and conceptually described in [6, 7], consists of applying a Gaussian noise (GN) stimulus to the input of the ADC and calculating the calibration-codes from the histogram of the output codes. There are several advantages when GN is used together with histogram-based calibration: the ADC can be seen as a "black-box" and does not need to be modified; GN, having a uniform power spectral density, allows full-speed dynamic calibration [8], and the use of a histogram eliminates uncertainties of the calibrating-codes due to noise.

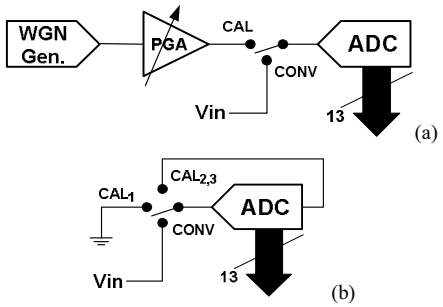

Figure 1. Calibration of ADCs using thermal noise. (a) Technique in [6, 7]; (b) Proposed new technique without Gaussian noise generator and PGA.

However, there are three drawbacks in the technique described in [6, 7]: 1) it requires two additional analogue blocks, namely a GN generator (GNG) and a programmable-gain amplifier (PGA) to adjust the standard-deviation (σ) of the GNG; 2) since the output histogram has a Gaussian shape, an internal table containing the ideal mathematically-produced histogram has to be stored in a memory; 3) the σ of the GNG has to be calibrated with reasonable accuracy before the calibration of the ADC itself.

The novel self-calibration technique proposed in this work is illustrated in Fig. 1(b). The main advantage is the absence of additional analogue blocks, since the internal thermal noise of the ADC is used. This low-amplitude noise is, in a first step (clock-cycle), successively amplified by the several residue amplifications of the MDACs in the pipeline chain. In a second clock-cycle, it is recycled, amplified again and folded several times. Due to the folding by the MDACs, the GN is

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converted into uniform noise (UN). In a third clock cycle, this noise is digitized by the ADC and a sample of the digital output is stored. After performing this 3-step procedure repeatedly, a histogram with many samples is obtained. Based on this histogram, a very simple digital-domain self-calibration algorithm can be applied. The calibrating-codes are obtained computing the deviations from uniformity of the noise in a small pre-defined number of bins.

This paper is organized as follows. In section II the overall architecture is described and the typical conversion characteristics of an ADC and of a pipelined stage are reviewed. Section III describes the proposed self-calibration technique. Section IV presents high-level simulation results, taking into account the most relevant non-ideal effects. Finally, section V draws the main conclusions.

II. ADC Architecture

The basic architecture is shown in Fig. 2. A front-end Sample-and-Hold (S/H) with a closed-loop gain of 2 is followed by a cascade of 3 equal 3.5-bit stages and by a last 4-bit flash quantizer. Each 3.5-bit stage has a 3.5-bit MDAC and a 3.5-bit quantizer. The 16 output bits provided by the four quantizers are then digitally synchronized and a net resolution of 13 bits is available after standard digital correction (summing all 4-bit words with 1-bit overlap). This architecture will be used, in section III, to describe the new self-calibration technique. Although 3.5-bit stages are used in this example, the technique can be generalised to any resolution *per* stage in a straightforward way.

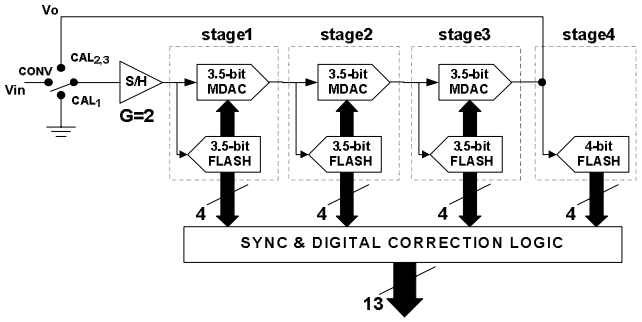

Figure 2. Architecture of the proposed 13-bit 4-stage pipeline ADC.

With this architecture the ADC overall non-linearities are limited mainly by the mismatches in the front-end 3.5-bit stage (specifically in the first 3.5-bit MDAC). The effect of errors caused by these mismatches in the conversion characteristic of the ADC is shown in Fig. 3(a). It consists of having 15 segments shifted (there are 14 jumps) and slightly rotated from the ideal straight line (dashed line). The gain-error of the 3.5-bit MDAC affects equally the slope of these segments and the shifts are due to the 14 non-linearity errors of the MDAC.

The third 3.5-bit stage has available an analogue output which drives the last 4-bit quantizer. As will be shown in the next section, this output will be useful to obtain the UN stimulus necessary for the new self-calibration algorithm. Note also that, as shown in Fig. 3(b), the typical transfer function of a 3.5-bit stage has a gain of 8 with 14 foldings and with the analogue output bound to ±0.5 LSB referred to 4 bits.

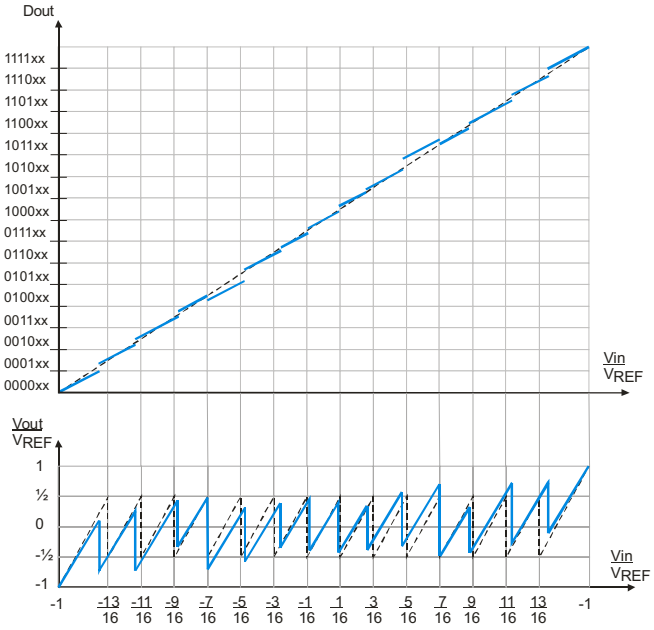

Figure 3. (a) Conversion characteristic of an 13-bit ADC with a 3.5-bit first stage with gain and non-linearity errors; (b) conversion characteristic of a 3.5-bit stage (dashed-line: ideal transfer function).

III. Proposed Self-Calibration Technique

The new self-calibration technique consists of applying a UN stimulus (internally generated) to the ADC and calculating the calibrating-codes from the histogram of the output codes. Each sample of the UN is obtained in three clock-cycles which are repeated to obtain a large number of samples.

1) In a first clock-cycle, the differential input is grounded (the 2 single-ended inputs are short-circuited to the input common-mode voltage). The internal thermal noise of the ADC (of the order of half LSB below the quantization noise) is amplified by the gain of the S/H ($G = 2$) and by the residue amplification gains of the three 3.5-bit stages, as shown in Fig. 4(a);

2) In a second clock-cycle, as shown in Fig. 4(b), the amplified thermal noise is recycled once, by connecting the differential output of the third stage (v_O) to the differential input of the S/H, and it is used as the new stimulus for the ADC. Signal v_O is already GN with very large amplitude;

3) Finally, in a third clock-cycle, the output of the third stage is kept connected to the input of the S/H as shown in Fig. 4(c). Due to the many amplifications and foldings caused by the three stages during the second clock-cycle, the amplified GN is converted into UN and an output sample can be acquired and stored.

After running acquiring many samples by performing these 3 clock-cycles repeatedly, a histogram can be obtained as shown in Fig. 4(d). Since there are only 14 jumps to be measured, only 14 bins, defined around the code-transitions of the first 3.5-bit stage need to be computed and stored. These 14 code transitions are ideally centred in codes 767, 1279,

1791, 2303, 2815, 3327, 3839, 4351, 4863, 5375, 5887, 6399, 6911, 7423. Therefore, a histogram $H(i)$ with 14 bins is obtained by counting the average of the number of occurrences of the output-codes inside these bins. Since, there are always random offsets in the threshold voltages of the comparators used in the 3.5-bit quantizers, the transition voltages change and a jump might be lost. A conservative binwidth equal to 64 codes is used to compute $H(i)$ to guarantee that all 14 jumps can be detected.

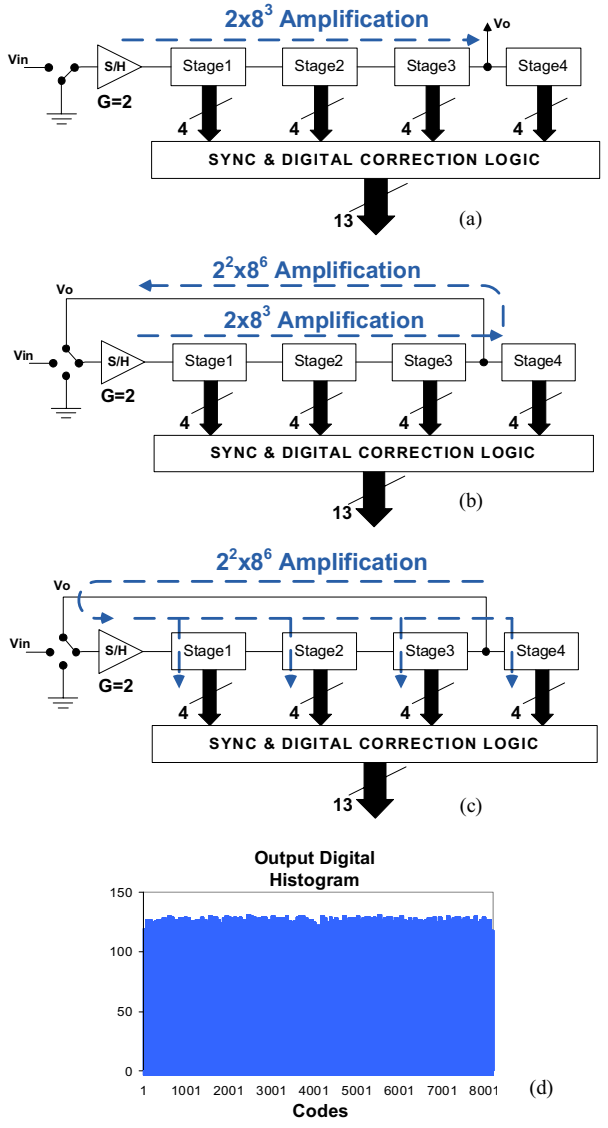

Figure 4. Three clock-cycles to obtain one sample of the histogram. (a) First clock-cycle and amplification by $2x8^3$. (b) Second clock-cycle, new amplification by 2^2x8^6 and foldings; (c) Third clock-cycle for digitization (a sample is obtained); (d) Histogram after obtaining many samples.

The obtained flat histogram with 14 bins deviates from the ideal one by the existing gain and non-linearity errors in the first 3.5-bit stage. For a large number of samples, n_S, the ideal flat histogram H_{ideal} would have $n_S / 2^{13}$ occurrences in every code. The 14 differences from this ideal value are used to calculate 15 (gain and non-linearity errors) calibrating codes. These are stored in a memory. During the normal conversion-mode, this memory is addressed by the first 3.5-bit quantizer and the 15 output calibrating codes are fetched and added to the un-calibrated 13-bit output.

The first step of the algorithm consists of determining the gain error present in all segments of the A/D conversion characteristic. Vector $D[i]$ can be calculated using

$$D[i] = (H[i] / H_{ideal} - 1) \cdot \text{binwidth} \qquad (1)$$

where i can vary from 1 to 15. With vector $D[i]$, it is possible to calculate the segment deviations from the ideal transfer characteristic. Since fully-differential MDACs exhibit code error symmetry, corresponding symmetric bins are added to eliminate possible errors caused by offset voltages in the amplifiers of the S/H and MDACs

$$D_S[i] = D[i] + D[16 - i]. \qquad (2)$$

where i can vary from 1 to 8. The 15 calibrating codes, *calcode*, can now be obtained according to:

$$calcode[1] = gain\_error = -0.5 \cdot \sum_{i=1}^{8} D_S[i] \qquad (3)$$

$$\begin{cases} calcode[i] = calcode[i-1] + 0.5 \cdot D_S[i-1], & 2 \le i \le 7 \\ calcode[i] = -calcode[16-i], & 9 \le i \le 15 \end{cases} \qquad (4)$$

Note that $calcode(8) = 0$ (always) and only elementary operations, namely addition, subtraction, multiplication by constants and division by powers of two are used. As a result the digital implementation is simple, and no multipliers are required.

III. Simulation Results

To assess the performance of the proposed technique, the 13-bit 4-stage pipeline ADC with the architecture in Fig. 1 was modelled using the C++ programming language. The main static non-ideal effects were included, namely finite gain in the amplifiers used in the S/H and MDACs (set to 77 dB), the offset voltages of these amplifiers and the offset voltages in the comparators of all quantizers, and mismatches in the capacitor-arrays of all 3.5-bit MDACs. Random mismatches with a standard deviation of 0.1 % (10-bit matching) were considered in all capacitances of the 3.5-bit MDACs, and random offsets with standard deviation of 2 mV were assumed in the threshold voltages of all comparators used in the quantizers.

The input-referred thermal noise of the ADC was set as 0.5 LSB below the quantization noise when taking into account the contributions from the S/H and all MDACs. If the ADC is properly designed this amount of noise ($\sigma_{\text{thermal rms}} \approx 1/7$ LSB) is enough for the correct operation of the algorithm. The clock RMS jitter was set to 2 ps. In order to extract the desired calibrating-codes, 2^{26} samples are found (empirically) to have enough statistical meaning. Figs. 5 and 6 show the histogram with binwidth=1 and with binwidth=64. As observed in these Figs., 14 different spikes appear in the code transitions of the first 3.5-bit stage. Using a binwidth of 64, these spikes have all information required to calculate the 15 calibrating codes according to the algorithm described in section III.

Figs. 7 and 8 show, respectively, the INL of the converter before and after calibration. The INL before calibration is between -4 and 4 LSB and after calibration is improved to about ±1 LSB. After calibration, the INL errors might exceed slightly the values of ±1 LSB since the second stage is not calibrated and, additionally, the calibrating codes are truncated.

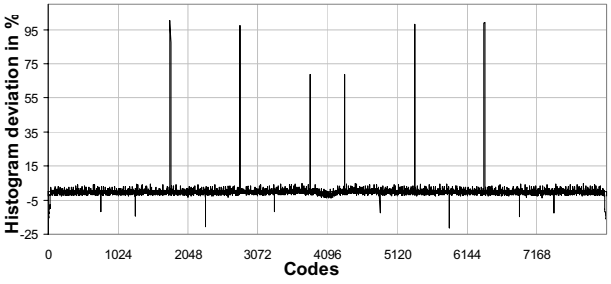

Figure 5. Normalized Histogram with *binwidth* = 1.

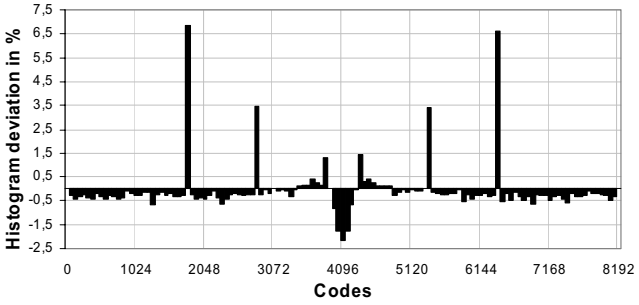

Figure 6. Normalized Histogram with *binwidth* = 64.

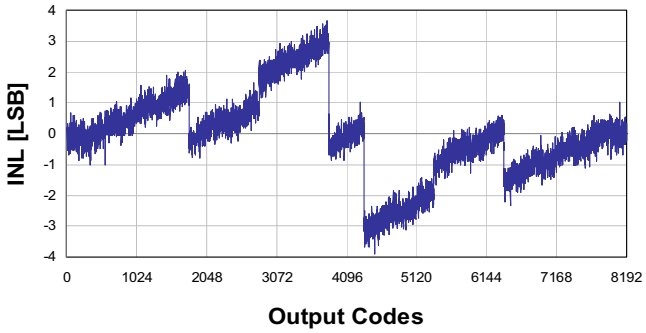

Figure 7. INL before calibration.

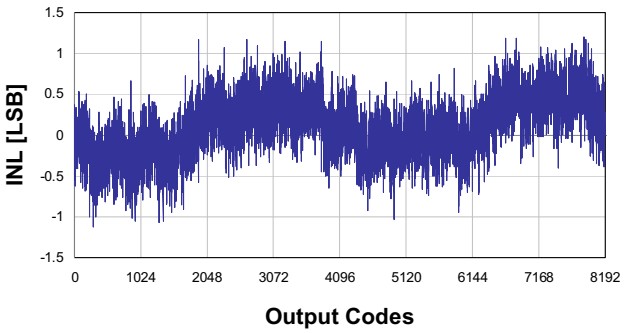

Figure 8. INL after calibration

The improvement in the dynamic performance of the ADC was demonstrated. Figs. 9(a) and (b) show the FFTs of the ADC output before and after calibration. The SFDR and the THD are improved from 75 dB and −71 dB to 81 dB and −79dB, respectively.

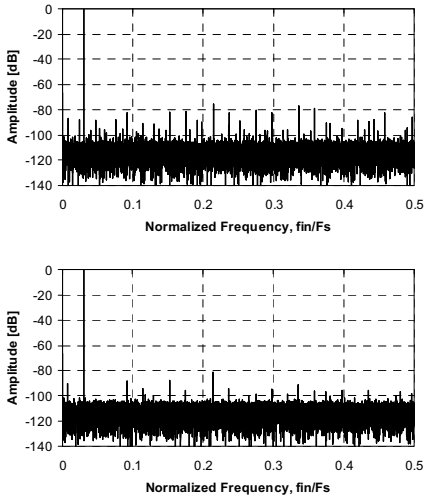

Figure 9. FFT of the output of the ADC. (a) before calibration. (b) after calibration.

IV. Conclusions

This paper described a new digital-domain self-calibration technique for high-speed pipeline A/D converters using the internal thermal noise as input stimulus. Simulated results of the calibration of a 13-bit pipeline ADC was shown, which demonstrated that both, static and dynamic linearity are significantly improved by using this technique.

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